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## 1.5-V CMOS Current Multiplier/Divider

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### ABSTRACT

A circuit technique for designing a compact low-voltage current-mode multiplier/divider circuit in CMOS technology is presented. It is based on the use of a compact current quadratic cell able to operate at low supply voltage. The proposed circuit is designed and simulated for implementing in TSMC 0.25- $\mu$ m CMOS technology with a single supply voltage of 1.5 V. Simulation results using PSPICE, accurately agreement with theoretical ones, have been provided, and also demonstrate a maximum linearity error of 1.5%, a THD less than 2% at 100 MHz, a total power consumption of 508  $\mu$ W, and -3dB small-signal frequency of about 245 MHz.

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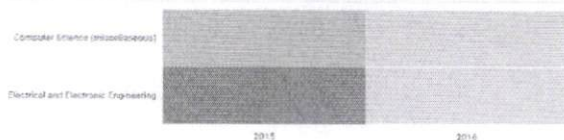
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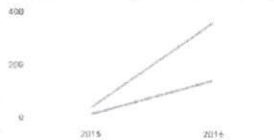
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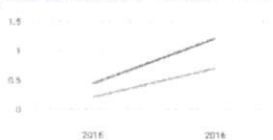
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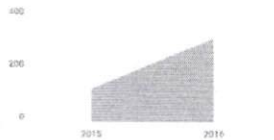
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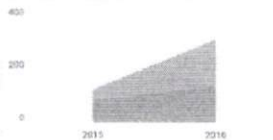
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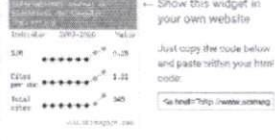
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